Ex parte Razden et al.

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAHUL RAZDAN and GABRIEL BISCHOFF

Appeal No. 96-3337
Application 08/019,574[1]

ON BRIEF

Before KRASS, JERRY SMITH and FLEMING, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 3, all of the claims pending in the application.

[1] Application for patent filed February 18, 1993.

The invention pertains to employing a pre-analysis and a two-state optimistic model to reduce computation in a transistor circuit simulation.

Independent claim 1 is reproduced as follows:

1. A method of reducing computational requirements for executing simulation code for a transistor circuit design having at least some elements which are synchronously clocked by multiple phase clock signals, the transistor circuit design being subject to resistive conflicts and to charge sharing, the simulation code including data structures associated with circuit modules and nodes interconnecting the circuit modules, the method comprising, by computer

generating a three-state version of simulation code for the transistor circuit design, said three-state version of simulation code having three states corresponding to states 0, 1, or X, where X represents an invalid or undefined state, said undefined state including representation of effects resulting from said resistive conflicts and said charge sharing,

performing a preanalysis of the three-state version of simulation code and storing phase waveforms each representing values occurring at a node of the transistor circuit design,

determining from said phase waveforms, each phase of a module for which no event-based evaluation need be performed,

storing for said each phase of a module for which no event-based evaluation need be performed, an appropriate response to an event occurring with respect to the module of the three state version of simulation code,

generating a two-state version of simulation code for the transistor circuit design, the two states corresponding to 0, and 1,

executing said two-state version of simulation code for each phase of a module for which no event-based evaluation need be performed, using as said data structures for said two-state version of simulation code the stored response from said three-state version of simulation code.

The examiner relies on the following reference:

Bryant, "Boolean Analysis of MOS Circuits," IEEE Transactions on Computer Aided Design, Vol. CAD-6, No. 4, pp. 634-649 (July 1987).

Claims 1 through 3 stand rejected under 35 U.S.C. 102(b) as anticipated by Bryant.

Reference is made to the brief and answer for the details of the respective positions of appellants and the examiner.

OPINION

We will not sustain the rejection of claims 1 through 3 under 35 U.S.C. 102(b) because, in our view, the examiner has failed in his burden to establish a prima facie case of anticipation.

Independent claim 1 requires, inter alia, in the "performing a preanalysis" step, "storing phase waveforms each representing values occurring at a node of the transistor circuit design." The examiner identifies this step in Bryant at page 637, col. 1 in the explanation of the rejection. More particularly, the examiner points to the "Steady-State" response detailed by Bryant at page 637, col. 2 in the response to appellants' arguments. At page 4 of the answer, the examiner states

> The claims have already defined "storing phase waveforms" to mean values "representing

> values occurring at a node of the transistor circuit design." Accordingly, there are no "phases" as in clock phases as it appears that Applicant is [sic, Applicants are] arguing [sic, arguing is] required by the claim language. The claim language requires that data be determined for each node in the design, which is the steady-state level determined by Bryant's preanalysis.

We find the examiner's reasoning to be flawed. Contrary to the examiner's assertion, claim 1 does not define the storing of phase waveforms as values "representing values occurring at a node of the transistor circuit design." Rather, the claim recites the storing of phase waveforms wherein each waveform represents values occurring at a node of the transistor circuit design. Such phase waveforms are required by the instant claims and Bryant discloses nothing with regard to such waveforms.

It may be that the steady-state level determined by Bryant's preanalysis determines data for each node of a transistor circuit design as alleged by the examiner, but there is no indication in Bryant that such data is in the form of phase waveforms as required by the instant claims. Merely because the prior art may perform the same or similar function as does the instant claimed invention does not mean that it inherently must perform that function in the same manner as the claimed invention.

Since Bryant fails to disclose any phase waveforms, as claimed, Bryant also cannot teach "determining from said phase

waveforms, each phase of a module for which no event-based evaluation need be performed," as claimed.

Further, claim 1 recites the generation of "a two-state version of simulation code for the transistor circuit design, the two state corresponding to 0, and 1" and "executing said two-state version of simulation code..." The examiner points to the table at page 638 of Bryant for such a teaching and states that "a two state model having only states 0 and 1 is derived from the three state model of the circuit" [bottom of page 5 of the answer]. However, in Bryant, each of the three states is represented by a two digit code made up of 0's and 1's, i.e., 1 is represented by 10, 0 is represented by 01 and X is represented by 11. This is not the same as "generating a two-state version of simulation code...the two states corresponding to 0, and 1," as claimed.

Still further, even assuming, arguendo, that the examiner's broad interpretation of the claim language in this regard is reasonable, we fail to see how Bryant discloses "executing said two-state version of simulation code for each phase of a module...using as said data structures for said two-state version of simulation code the stored response from said three-state version of simulation code," required by the instant claims. The examiner's reference to pg. 634, col. 2 "A. New Approach" of Bryant [page 6 of the answer] for support of his

position that Bryant does disclose what is claimed is unpersuasive as we find nothing therein which teaches "executing said two-state version of simulation code for each phase of a module...using as said data structures for said two-state version of simulation code the stored response from said three-state version of simulation code."

While Bryant and the instant claims are clearly directed to similar subject matter, the examiner has not convinced us that they are performing the same function in the same manner and we will not resort to speculation in order to sustain a rejection based on anticipation under 35 U.S.C. 102.

Accordingly, the examiner's decision rejecting claims 1 through 3 under 35 U.S.C. 102(b) as anticipated by Bryant is reversed.

REVERSED

ERROL A. KRASS)
Administrative Patent Judge)
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JERRY SMITH) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
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